



LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS)  
Accredited by NAAC & NBA (Under Tier - I) and ISO 9001:2015 Certified Institution Approved  
by AICTE, New Delhi and Affiliated to JNTUK, Kakinada  
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

## REPORT

on

### **AICTE Sponsored Online Short Term Training Program**

on

### **“Mixed Signal Design Approaches for Artificial Intelligence Processors” Series – 3 (1<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)**

Department of ECE of Lakireddy Bali Reddy College of Engineering (Autonomous), has organized AICTE Sponsored Online Short Term Training Program (STTP) on “Mixed Signal Design Approaches for Artificial Intelligence Processors” under the coordinator-ship of Dr. Srinivasulu Gundala. The Program was conducted as Series - 3 of three series scheduled from **01-03-2021 to 06-03-2021**.

#### **ABOUT AICTE – STTP:**

All India Council for Technical Education (AICTE) was set up in November 1945 as a national-level apex advisory body to conduct a survey on the facilities available for technical education and to promote development in the country in a coordinated and integrated manner. And to ensure the same, as stipulated in the National Policy of Education (1986), AICTE was vested with: Short Term Training Program (STTP) intends to conduct faculty trainings through financial assistance from AICTE to enable faculty members in the field of technical education to introspect and learn techniques that can help prepare students for active and successful participants in a knowledge society.

#### **OBJECTIVES of STTP:**

The objectives of the training program are:

- ❖ To alleviates the Design and analysis of Energy efficient Voltage & Data converters, Behavioral modeling of Analog and Mixed signal IC
- ❖ To Design aspects of Analog and Mixed Signal IC, Case studies on RF IC and AI Processors.
- ❖ To provides platform to enhance the skills towards Design and development of intelligent computational systems for the Teaching faculty.

#### **Date: 1<sup>st</sup> March 2021**

#### **Inauguration:**

STTP was inaugurated on 1<sup>st</sup> March 2021 at 9:30 AM by **Dr. Y. Amar Babu**, HOD of ECE and Convener of STTP along with chief guest of the programme Dr. Hitesh Shrimali, Associate Professor, School of Computing and Electrical Engineering, IIT Mandi, Principal of LBRCE **Dr. K. Appa Rao**, and Coordinator of STTP **Dr. Srinivasulu Gundala**.

**Dr. Srinivasulu Gundala**, has welcomed all the delegates and participants to the STTP. In his speech, he highlighted the main objectives and importance of this Short-Term Training Programme. Along with this, he gave a brief introduction about selection process and eligibility for awarding the certificate.



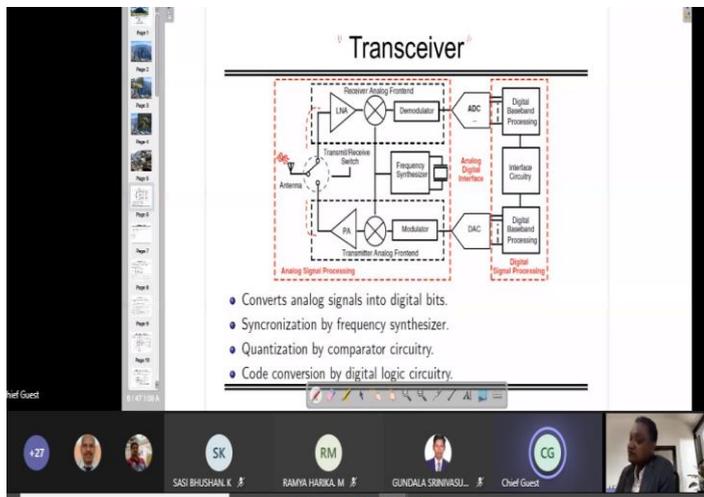
**Welcome  
to  
AICTE  
Sponsored Online  
Short Term Training Program on  
"Mixed Signal Design Approaches  
for Artificial Intelligence  
Processors"  
Series-3  
(1<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)**



**Day 1: 1<sup>st</sup> March 2021 [FN]**

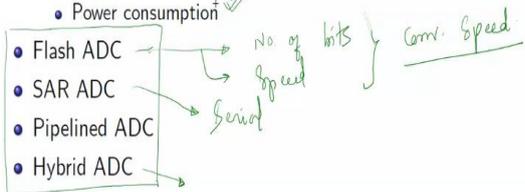
**Topic : Design and Modelling of Energy efficient Hybrid Data Converters**  
**Resource Person : Dr. Hitesh Shrimali, Associate Professor, School of Computing and Electrical Engineering, IIT Mandi**

The resource Person Dr. Hitesh Shrimali, Associate Professor, School of Computing and Electrical Engineering, IIT Mandi, started his presentation by giving design challenges for low-power CMOS high-speed analog-to-digital converters (ADCs), basic ADC converter architectures are described with particular focus on their suitability for the construction of power-efficient hybrid ADCs. Highlighted the key concepts of Low resolution ADCs, which can be employed to improve the energy efficiency (EE) of a wireless receiver since the power consumption of each ADC is exponentially related to its sampling resolution and the hardware complexity.



**Selection of ADC**

- The analog-to-digital converter (ADC) topology is chosen carefully to achieve the desired trade off between
  - Number of bits, ↓
  - Sampling rate and ↓
  - Power consumption ↑



**Day 1: 1<sup>st</sup> March 2021 [AN]**

**Topics : Case studies on VLSI Architectures for Mixed signal applications.**  
**Resource Person : Dr. Saila Subbaraman, Dept. of ECE, WCE, Sangli**

The resource Person **Dr. Saila Subbaraman**, Dept. of ECE, WCE, Sangli has discussed about emerging applications and address on recent breakthroughs in the VLSI architecture design for DSP, including design and analysis of signal processing algorithms and architecture, performance analysis of signal processing systems, VLSI design methodology, design of arithmetic circuits and VLSI components used in signal processing. The high integration of system ICs has large silicon areas of digital blocks. However, the analog and mixed-signal blocks are still the bottleneck of the VLSI implementation due to nature of the analog design works.



**AICTE Sponsored STTP on  
"Mixed Signal Design Approaches for Artificial Intelligence Processors"**

**Series - 3  
(01<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)  
DAY - 1 (01-03-2021)  
Session - 2 (AN) 02:00 PM to 04:00 PM**

**Resource Person  
Dr. Saila Subbaraman, Dept. of ECE, WCE, Sangli**



**Topics**

Case studies on VLSI Architectures for Mixed signal applications

## Organization

- **Overview of DSP** Part I
  - Objectives of DSP
  - Typical DSP Computations
- **DSP Architectures**
- **FPGA technology**
- **CORDIC Processor** Part II
  - Concept, Implementation
- **Summary and Conclusions**

Dr S. Subbaraman, Ex-Professor,  
WCE, Sangli

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### Day 2: 2<sup>nd</sup> March 2021 [FN]

**Topics : Challenges in mixed signal design**

**Resource Person : Dr. Rakesh Kumar P., Dept. of Electrical Engineering, IIT Delhi**

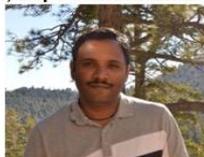
The resource Person Dr. Rakesh Kumar, Dept. of Electrical Engineering, IIT Delhi, started his demonstration by giving today's on-chip Analog/Mixed-Signal and RF (A/RF) systems have reached a limit of size and complexity where transistor-level SPICE and Fast SPICE simulation approaches cannot deliver a verification solution on time. Challenges include, of course, circuit size, but also the heterogeneous nature of the A/RF systems, their architectural complexity and demanding specifications. Such challenges can only be surmounted by moving to a level of abstraction above that of the transistor. The benefits of this approach are illustrated with examples based on new tools that work at the Analog System Implementation (ASI) level of abstraction and which favor schematic, rather than language-based, descriptions of the A/RF system.



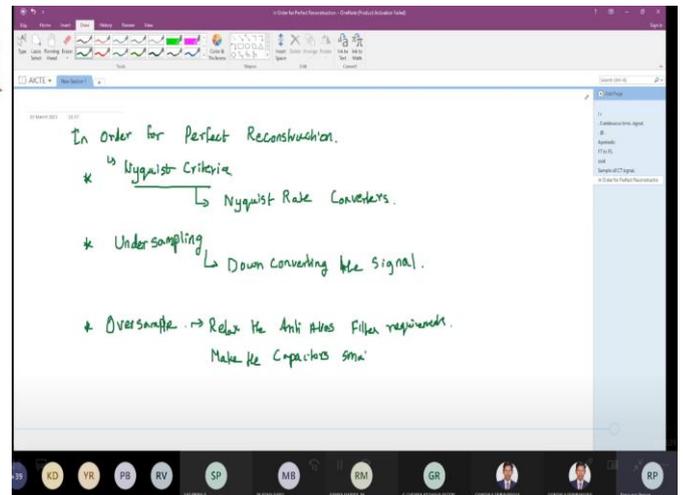
**AICTE Sponsored STTP on  
"Mixed Signal Design Approaches for Artificial Intelligence Processors"**

**Series - 3  
(01<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)  
DAY - 2 (02-03-2021)  
Session - 1 (FN) 10:00 AM to 12:00 PM**

**Resource Person  
Dr. Rakesh Kumar, Dept. of Electrical Engineering, IIT Delhi**



Topic: Challenges in mixed signal design



### Day 2: 2<sup>nd</sup> March 2021 [AN]

**Topics : Case studies on Mixed signal techniques based Machine learning system**

**Resource Person : Dr. Sakthivel R., School of Electronics Engineering, VIT Vellore**

The resource Person Dr. Sakthivel R., School of Electronics Engineering, VIT Vellore, explored insights of Artificial intelligence methods used in different interdisciplinary areas. The method of machine learning and data mining for testing and fault diagnostics in analog/mixed-signal integrated circuits. The case study results for analog filters are demonstrated and discussed. The proposed method and approach can be used according to the design-for-testability flow for analog/mixed-signal integrated circuits.



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Session - 2 (AN) 02:00 PM to 04:00 PM

Resource Person  
Dr. Sakthivel R., School of Electronics Engineering, VIT Vellore



Topic: Case studies on Mixed signal techniques based Machine learning system

### Spiking Thresholds and Refractory Periods

Voltage-amplifier I&F neuron. (a) Schematic diagram; (b) membrane voltage trace over time

### Day 3: 3<sup>rd</sup> March 2021 [FN]

Topics : Deep neural networks and case study in computer vision

Resource Person : Dr. Mohamed Faruk, Dept. of ECE, NIT Warangal

The resource Person Dr. Mohamed Faruk, Dept. of ECE, NIT Warangal, started his discussion on the field of study on deep neural networks, enabling machines with its own ability called Computer Vision (CV). CI and AI models to recognize anything in visual data – objects, concepts, faces, and actions. That's AI computer vision. AI currently has deployed over 2,400 AI models. Number of patented Dense Classification image analysis enables contextual perceptions which are modeled after human visual perception. By understanding context, how AI can select the appropriate models and type of search to return faster results with higher accuracy. This capability provides computer vision with speed, accuracy, flexibility and scaling.



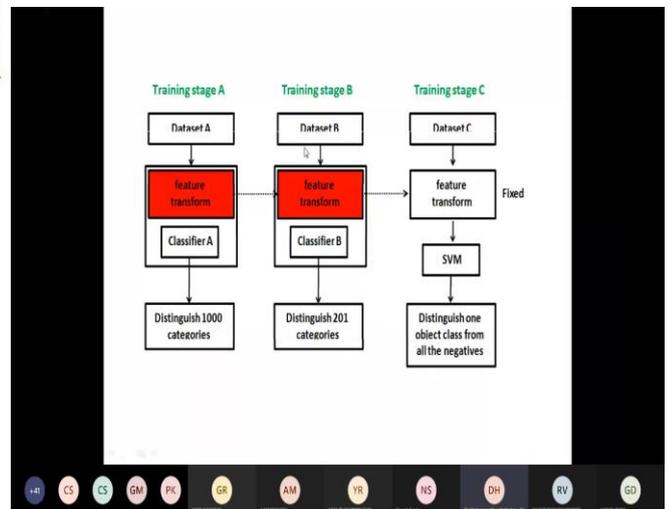
AICTE Sponsored STTP on  
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Series - 3  
(01<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)  
DAY - 3 (03-03-2021)  
Session - 1 (FN) 10:00 AM to 12:00 PM

Resource Person  
Dr. Mohamed Faruk, Dept. of ECE, NIT Warangal



Topic: Deep neural networks and case study in computer vision



### Day 3: 3<sup>rd</sup> March 2021 [AN]

Topics : Neural networks and Machine Learning Algorithms

Resource Person : Mrs. Lyla B. Das, Dept. of ECE, NIT Calicut

The Resource Person Mrs. Lyla B. Das, Dept. of ECE, NIT Calicut, in his lecture described about machines learning algorithms. Machines have brains; their brains are able to solve the sorts of problems that, until recently, humans were uniquely good at. Neural networks, as the name suggests, are modeled on neurons in the brain. They use artificial intelligence to untangle and break down extremely complex relationships. Neural networks are one of the learning algorithms used within machine learning. They consist of different layers for analyzing and learning data. Every hidden layer tries to detect patterns on the picture. When a pattern is detected the next hidden layer is activated.



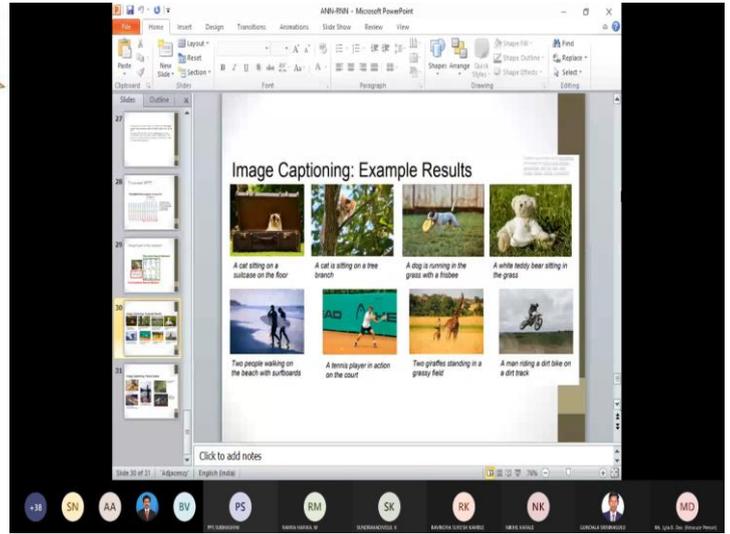
**AICTE Sponsored STTP on  
"Mixed Signal Design Approaches for Artificial Intelligence Processors"**

**Series - 3  
(01<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)  
DAY - 3 (03-03-2021)  
Session - 2 (AN) 02:00 PM to 04:00 PM**

**Resource Person  
Mrs. Lyla B. Das, Dept. of ECE, NIT Calicut**



**Topic: Neural networks and ML Algorithms**



**Day 4: 4<sup>th</sup> March 2021 [FN]**

**Topics : Power management strategies for Mixed signal circuits**  
**Resource Person : Dr. K. Venkata Ramanaiah, Dept. of ECE, Yogi Vemana University**

The resource person Dr. K. Venkata Ramanaiah, Dept. of ECE, Yogi Vemana University, in his presentation discusses on analog DFT techniques and methodologies used in integrated power management (PM) systems to overcome challenges of mixed-signal SoC qualification. Systems on Chip (SoC) designs today have a large number of power domains regulated by complex on-chip power management logic. The power management logic is primarily digital in nature, but it relies on analog components such as Low Dropout Regulators (LDO) and Phase-Locked Loops (PLL) for delivery of regulated voltages and clock frequencies. In low power designs, such analog components may also be powered down at times, and hence power domains are defined around modules containing these components. The digital brain of the power management logic must correctly consider the latencies of the analog components in the power management fabric while switching the power domains driven by these components.



**AICTE Sponsored STTP on  
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**Series - 3  
(01<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)  
DAY - 4 (04-03-2021)  
Session - 1 (FN) 10:00 AM to 12:00 PM**

**Resource Person  
Dr. K. Venkata Ramanaiah, Dept. of ECE, Yogi Vemana University**



**Topic: Power management strategies for Mixed signal circuits and Case studies**



**Day 4: 4<sup>th</sup> March 2021 [AN]**

**Topics : Compact Modeling of Semiconductor devices**  
**Resource Person : Dr. Chandan Yadav, Dept. of ECE, NIT Calicut**

Dr. Chandan Yadav Dept. of ECE, NIT Calicut, started the discussion on Compact Model development of semiconductor devices. Semiconductor device modeling creates models for

the behavior of the electrical devices based on fundamental physics, such as the doping profiles of the devices. His presentation highlights are device physics, partition model specific regions and assign EC elements, element formulation and error determination, modified nodal analysis to implement compact model and model testing for extreme bias/parameter combinations. Model customization for foundry for test-structure preparation, characterization, parameter extraction, model validation and design kit preparation for specific EDA tool.



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**Series - 3**  
**(01<sup>st</sup> March 2021 to 6<sup>th</sup> March 2021)**  
**DAY - 4 (04-03-2021)**  
**Session - 2 (AN) 02:00 PM to 04:00 PM**

**Resource Person**  
**Dr. Chandan Yadav, Dept. of ECE, NIT Calicut**



**Topic: Compact Modeling of Semiconductor devices**

From charge neutrality we can write

$$Q_c = q(p - n + N_D - N_A) \quad (3)$$

Using Fermi-Dirac statistics ( $f_{FD}$ )

- mobile electron charge (n)
- mobile hole charge (p)

$$n = q \int_{E_c}^{\infty} \rho_{DOS}(E) f_{FD}(E) dE \quad (4)$$

$$p = q \int_{-\infty}^{E_v} \rho_{DOS}(E) (1 - f_{FD}(E)) dE \quad (5)$$

where,

$$\rho_{DOS}(E) = \frac{g_v g_c m_e^*}{2m^3}$$

$$f_{FD}(E) = \frac{1}{1 + \exp\left(\frac{E - E_f}{kT}\right)}$$

and

$$n = q \int_{E_c}^{\infty} \rho_{DOS}(E) \ln\left(1 + \exp\left(\frac{E_f - E}{kT}\right)\right) dE \quad (6)$$

where,

$$\rho_{DOS}(E) = \frac{g_v g_c m_h^*}{2m^3}$$

$\rho_{DOS}$  → Density of states (DOS) for electrons  
 $\rho_{DOS}$  → Density of states (DOS) for hole  
 $E_c$  → Minima of conduction band  
 $E_v$  → Maxima of valance band  
 $m_e^*$  → electron effective mass  
 $m_h^*$  → hole effective mass

**Day 5: 5<sup>th</sup> March 2021[FN]**

**Topics : Supervised and unsupervised learning algorithms**

**Resource Person : Dr. Varun Gopi, Dept. of ECE, NIT Tirucharapalli**

The resource Person Dr. Varun Gopi, Dept. of ECE, NIT Tirucharapalli, in his lecture explained about the supervised learning, unsupervised learning algorithms and the classification and regression supervised learning problems, about the clustering and association unsupervised learning problems. Good number of example based algorithms used for supervised and unsupervised problems. A problem that sits in between supervised and unsupervised learning called semi-supervised learning.



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**DAY - 5 (05-03-2021)**  
**Session - 1 (FN) 10:00 AM to 12:00 PM**

**Resource Person**  
**Dr. Varun Gopi, Dept. of ECE, NIT Tirucharapalli**



**Topic: Supervised and unsupervised learning algorithms**

### Classification

- Learning (training):** Learn a model using the training data.
 

Model construction: describing a set of predetermined classes. Each tuple/sample is assumed to belong to a predefined class, as determined by the class label. The set of tuples used for model construction is the training set.
- Testing:** Test the model using unseen test data to assess the model accuracy.
 

Model usage: for classifying future or unknown objects. If the accuracy is acceptable, use the model to classify data tuples whose class labels are not known.

```

    graph LR
      A[Training data] --> B[Learning algorithm]
      B --> C[model]
      C --> D[Test data]
      D --> E[accuracy]
      subgraph Step 1
        A
        B
        C
      end
      subgraph Step 2
        D
        E
      end
    
```

**Day 5: 5<sup>th</sup> March 2021[AN]**

**Topics : Design aspects of analog and mixed signal ICs**

**Resource Person : Dr. Saurabh Kumar Pandey, Dept. of Electrical Engineering, IIT Patna**

The resource Person Dr. Saurabh Kumar Pandey, Dept. of Electrical Engineering, IIT Patna, given demonstration on the Modern ICs, the modern ICs are often composed of elements from each domain. This is increasingly the case with compact and sophisticated wireless communications and sensing hardware, such as automotive radar, where a single device performs a wide range of sensing, processing, conversion, mathematical manipulation, storage, decision making, and communication. These mixed-signal designs usually involve several teams that must work with some unifying EDA tool that ensures each aspect of the design follows process constraints. This is increasingly important as SoCs.



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**DAY - 5 (05-03-2021)**  
**Session - 2 (AN) 02:00 PM to 04:00 PM**

**Resource Person**  
**Dr. Saurabh Kumar Pandey, Dept. of Electrical Engineering, IIT Patna**



**Topic: Design aspects of analog and mixed signal ICs**

**System Domain**

Integrated circuit design:

- Complex activity
- Well-defined process
- The system is divided into functional blocks (subsystems)
- Defined first with respect to their interfaces between each other
- A series of design steps each follow modeling the results
- Simulation of the model assures the design meets the requirements

Hardware System

Iterative Design Process

**Day 6: 6<sup>th</sup> March 2021[FN]**

**Topics : Design strategies for Low power analog IC design**

**Resource Person : Dr. Mudasar Bashir, Infineon Technologies, Austria**

The resource Person Dr. Mudasar Bashir, Infineon Technologies, Austria, in his discussion described about Design strategies for analog integrated circuits for the reduction of stochastic errors and systematic errors are normally not consistent with design strategies which take into account power dissipation, voltage range and current range. The combination of transfer quality, low voltage and low power must be considered during the whole design process. There are good reasons to choose current as the information-carrying quantity in the case of low-voltage low-power design constraints. He focuses on the influence of the transfer quality on that choice. To obtain power-efficient transfer quality, indirect feedback is shown to be a good alternative to traditional feedback techniques.



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**DAY - 6 (06-03-2021)**  
**Session - 1 (FN) 10:00 AM to 12:00 PM**

**Resource Person**  
**Dr. Mudasar Bashir, Infineon Technologies, Austria**



**Topic: Design strategies for Low power analog IC design**

**Comparison between three OTAs**

Parameter	(Sub-threshold; Gate-driven)	(Bulk-driven)	(Gain-boosted; Gate-driven)
CMOS technology	180 nm	180 nm	65 nm
Power Supply	0.5 V	0.5 V	1 V
DC gain	73 dB	78 dB	64.5 dB
Phase Margin	75 deg.	68 deg.	88 deg.
GBW	12.7 kHz	34 kHz	10 MHz
Slew Rate	10.8 V/msec	3.8 V/msec	17 V/μsec
Output capacitance	15 pF	15 pF	5 pF
Eq. input noise	216 nV/√Hz	1.6 μV/√Hz	0.16 nV/√Hz
Power consumption	64 nW	35 nW	12 μW
FoM <sub>GBW</sub>	297 HzF/W	1457 HzF/W	416.6 HzF/W
FoM <sub>SR</sub>			1125 VHzF/W



**Day 6: 6<sup>th</sup> March 2021[AN]**

**Topics : Architecture Exploration of AI and ML processors**  
**Resource Person : Dr. Srinivas Boppu, School of Electrical sciences, IIT Bhubaneswar**  
The resource Person Dr. Srinivas Boppu, School of Electrical sciences, IIT Bhubaneswar, in his lecture described about RL & Deep Learning: Deep reinforcement learning is the combination of reinforcement learning (RL) and deep learning. This field of research has been able to solve a wide range of complex decision-making tasks that were previously out of reach for a machine. Thus, deep RL opens up many new applications in domains such as healthcare, robotics, smart grids, finance, and many more. This manuscript provides an introduction to deep reinforcement learning models, algorithms and techniques. Particular focus is on the aspects related to generalization and how deep RL can be used for practical applications. We assume the reader is familiar with basic machine learning concepts.



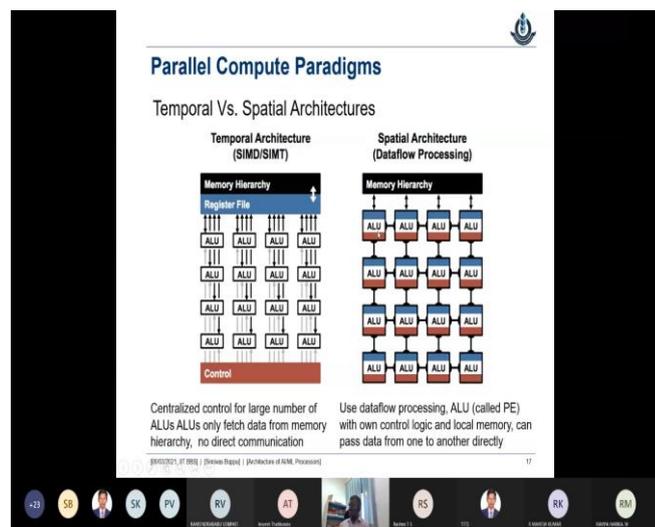
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DAY - 6 (06-03-2021)  
Session - 2 (AN) 02:00 PM to 04:00 PM**

**Resource Person  
Dr. Srinivas Boppu, School of Electrical sciences, IIT Bhubaneswar**



**Topic: Architecture Exploration of AI and ML processors**



**Parallel Compute Paradigms**  
Temporal Vs. Spatial Architectures

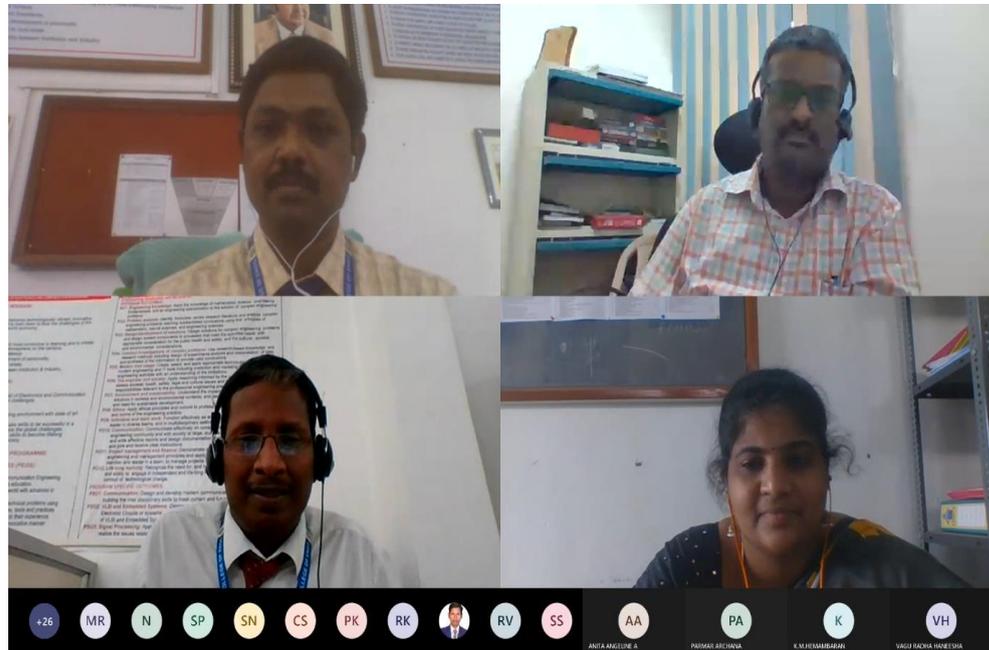
**Temporal Architecture (SIMD/SIMT)**  
Memory Hierarchy: Register File, ALU, ALU, ALU, ALU, ALU, ALU, ALU, ALU, ALU, Control.

**Spatial Architecture (Dataflow Processing)**  
Memory Hierarchy: ALU, ALU.

Centralized control for large number of ALUs. ALUs only fetch data from memory hierarchy, no direct communication.  
Use dataflow processing. ALU (called PE) with own control logic and local memory, can pass data from one to another directly.

**Date: 6<sup>th</sup> March 2021: Valedictory Session:**

STTP Valedictory Session held on 6<sup>th</sup> March 2021 at 3:45 PM by Coordinator of STTP **Dr. Srinivasulu Gundala**, Convener of STTP **Dr. Y. Amar Babu** along with Principal of LBRCE **Dr. K. Appa Rao**, chief guest of the programme **Dr. Srinivas Boppu**, School of Electrical sciences, IIT Bhubaneswar, and Participants.



A screenshot of a Zoom meeting showing four participants in a grid view. The participants are: a man in a yellow shirt (top left), a man in a checkered shirt with a headset (top right), a man in a white shirt with a headset (bottom left), and a woman in a dark top (bottom right). The Zoom control bar at the bottom shows icons for mute, video, chat, and other participants.

Dr. K. Appa Rao in his valedictory addressing, conveyed his wishes to all the participants of STTP, congratulated the Program Convener Dr. Y. Amar Babu and Coordinator Dr. Srinivasulu Gundala for organizing the STTP in a successful manner. Further, he appreciated all the Teaching and Non-Teaching Staff Members of ECE Department for promoting such kind of development programme. He also motivated to keep learning new technologies coming in future for the career growth as well as organizational growth.

At the end of the valedictory session, vote of thanks was given by Dr. Srinivasulu Gundala, Coordinator of the STTP in which he has been paid his gratitude to AICTE for sponsoring the STTP program, resource persons for spending valuable time for our participants and sharing the knowledge and all the participants for attending this STTP.

Expressed the gratitude to the **LBRCE management**, Principal **Dr. K. Appa Rao**, Dean R & D **Dr. E. V. Krishna Rao** and team, Teaching and non-teaching staff members of ECE dept. and Microsoft Teams online software providers for extending support and for providing us with an environment to complete STTP program successfully.

### **Feedback from the Participants:**

The feedback of the participants was very positive and motivational for the organizers. The participants felt very happy for conducting the STTP on latest trends in Industry. They said that, this program was very useful and helpful for them in their research, in turn guiding students in latest technologies. All the participants appreciated the sessions organized by the department of ECE and the arrangements made by the organizers.

The number of Online registrations by the Faculty members and Research scholars of AICTE approved institutions were 152, on an average 86 participants participated in online sessions, based on the eligibility criteria of the AICTE norms the e-certificates were issued to 70 participants.

15.03.2021



**Coordinator**  
**(Dr. Srinivasulu Gundala)**



**Convener**  
**(Dr. Y. Amar Babu)**